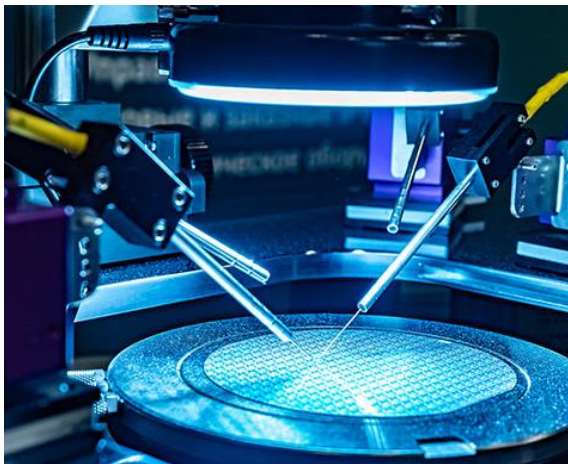


Piezoelectric Actuators in the Semiconductor Manufacturing Industry

Author: Jonathan Cali

Executive Summary:

This paper summarizes the significance of piezoelectric technology in the global semiconductor industry with a special focus on the manufacturing steps needed to produce every major silicon product: silicon wafers, silicon dice, and packaged silicon devices. An overview of the semiconductor manufacturing process is given, as well as the basics of piezo theory, and US/EU/Asian market studies. Wafer fabrication processes that utilize piezoelectric systems include wafer slicing and polishing. Piezoelectric systems are utilized in the following front-end processes: Chemical vapor deposition, mask inspection, defect inspection, and E-beam inspection. Finally, piezoelectric systems are especially useful in the back-end, specifically advanced packaging that include hidden surface cleaning and wire bonding. The intended audience of this technical whitepaper is someone actively working in the semiconductor industry who can utilize the addition of piezoelectric technology in their company and as an overview for someone with limited knowledge of the industry. This paper concludes with the importance for piezo manufactures and semiconductor manufacturers to collaborate in order to solve current and future manufacturing challenges.



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I. Introduction

A. Overview of the Semiconductor Industry

The semiconductor industry stands at the forefront of computational innovation, allowing advancements in information processing, communication, and numerous emerging technologies such as artificial intelligence and electric vehicles. This industry is a global market influenced by geopolitical relationships, supply chain intricacies, and rapidly evolving consumer demand. Starting with the development of the transistor, often deemed the most important invention in the modern age, the semiconductor industry has grown to impact nearly every single electronic device used today¹. Semiconductor chips can be found in nearly all markets including consumer electronics, healthcare, military, and automotive markets to name a few. The continuous advancement in this industry requires an increasingly important focus on manufacturing robustness and precision, a challenge piezoelectric system have seen success addressing.

Fundamentally, a semiconductor is a material that bridges the gap between insulators that inhibit the flow of electricity due to high resistivity and conductors that encourage the flow of electricity with high conductivity. Compared to traditional charge-carrying metals, semiconducting materials offer precise electrical conductivity control, device miniaturization, and energy efficiency. Germanium, aluminum nitride, and gallium arsenide have been proposed as the leading semiconductor materials; however, silicon has been the preferred material due to availability, cost, and superior performance characteristics.

Within this industry, the following terminologies are crucial to understand:

- Transistor: The most fundamental semiconductor device to switch and amplify electronic signals.
- Wafer: A thin slice of semiconductor material grown from crystallized silicon used for die fabrication.
- Die: A flat piece of semiconducting material where integrated circuits are fabricated. Individual dies are cut from semiconducting wafers.
- Chip: Often called an integrated circuit (IC), chips are packaged dice that include circuit framing, epoxy, or other additional materials. Chips are used in everyday items such as computers, electric vehicles, and servers.

The manufacturing process of semiconductor chips is complex and includes many interconnected steps, sometimes repeated, that form the desired semiconductor device. This process can split into three stages: Silicon wafer fabrication, front-end die fabrication, and back-end device packaging. Each stage

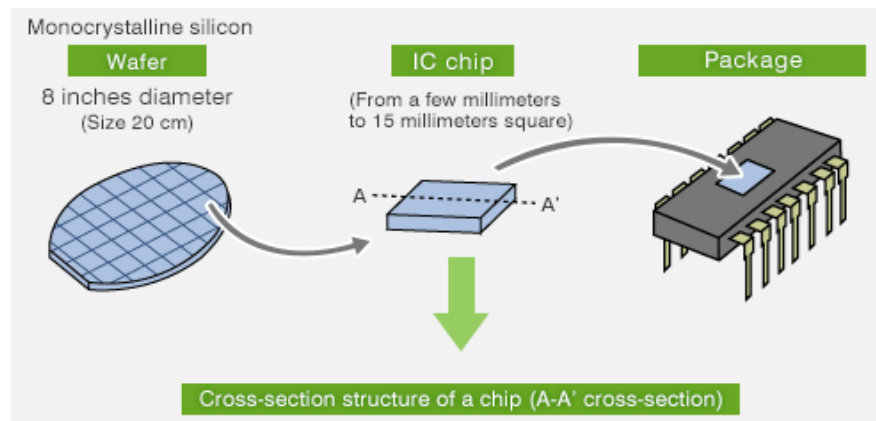


Figure (1) An 8-inch wafer is shown with cross-sections including individual die on the wafer. Each one of these dice are roughly 1 mm square and packaged into a device up to 10x the dice dimensions or more.

¹ ("Transistors- The Invention That Changed the World")

has unique challenges and production steps that require innovative solutions. One challenge is evident across all manufacturing steps: The impact due to the demand for smaller, denser, and faster chips.

B. Importance of Precision and Miniaturization in Semiconductor Manufacturing

This demand has caused an industry-wide focus on miniaturization that encourages cost reduction and process improvements that define the semiconductor industry. Moore's Law, named after Gordon Moore who was an Intel engineer and businessman, states that the transistor count on an integrated circuit doubles every two years. This law has held up until recently, as transistor sizes have approached the size of a few atoms wide, challenging the laws of molecular physics². The main concern is quantum tunneling, which disrupts the insulating/conducting properties of neighboring atoms within the transistors. This phenomenon only occurs at sub-nanometer scales and has not been a previous concern.

At a glance, the push for smaller and faster chips appears predictable since technological advancements typically equate to performance increases with smaller form factors. The market demand for faster, smaller, and more economical electronic devices supplements this observation. However, the mechanics behind chip miniaturization are much more nuanced. It may be intuitive to assume that increasing transistor quantity and size increases computational power when spaced traditionally. Although equally spaced transistors lead to increased power, the physical interconnections are longer which increases heat generation while decreasing power efficiency. Therefore, an alternate solution is needed to build complex modern devices and is solved by increasing transistor density. Not only does increasing transistor density save space by minimizing path length but it also reduces operational voltages, thus improving power efficiency. This way a single transistor-dense chip produces more computation operations at cooler temperatures and less power than a less transistor-dense chip twice its size.

Current semiconductor equipment and future innovations require precise and reliable equipment to address the continuing push for miniaturized chips and increasing chip demand. This whitepaper dives into the pivotal role piezoelectric systems play in solving these challenges so that the semiconductor industry can continue to be at the forefront of innovation and advancements in new technologies.

II. Market Overview of the Semiconductor Industry

A. Current Trends

As the semiconductor industry advances, micro and macro-level trends emerge that profoundly shape the industry. This is most evident with the industry's emphasis on supply chain diversification. The need for adaptable, flexible supply chain solutions has become necessary due to the following global trends:

- **Geopolitical Factors:** The quest for worldwide chip dominance has led to tensions between world leaders to develop robust and fast semiconductor infrastructure. US-China trade tensions are one example that highlights how current competition and future tensions could disrupt the world's supply of silicon chips. With increased tensions, trade restrictions could occur which reduces the availability of semiconductor devices, increase prices, and inhibit innovation. Therefore, semiconductor companies and other world leaders are placing a larger emphasis on supply chain diversification to bolster domestic manufacturing in their respective nations.

² (Moore)

- COVID-19 and Demand Surge: The COVID-19 pandemic highlighted the need for resilient supply chains. Sudden spikes in demand for electronics, coupled with disruptions due to workforce delays, caused significant chip shortages, emphasizing the need to have more diversified and adaptable supply chains. The industry responded by diversifying investments globally and enhancing workforce education.

Advanced packaging solutions have emerged to address continued chip miniaturization that goes beyond traditional methods to connect and package integrated circuits. These solutions offer new methods to pack components into smaller footprints to enhance performance and functionality:

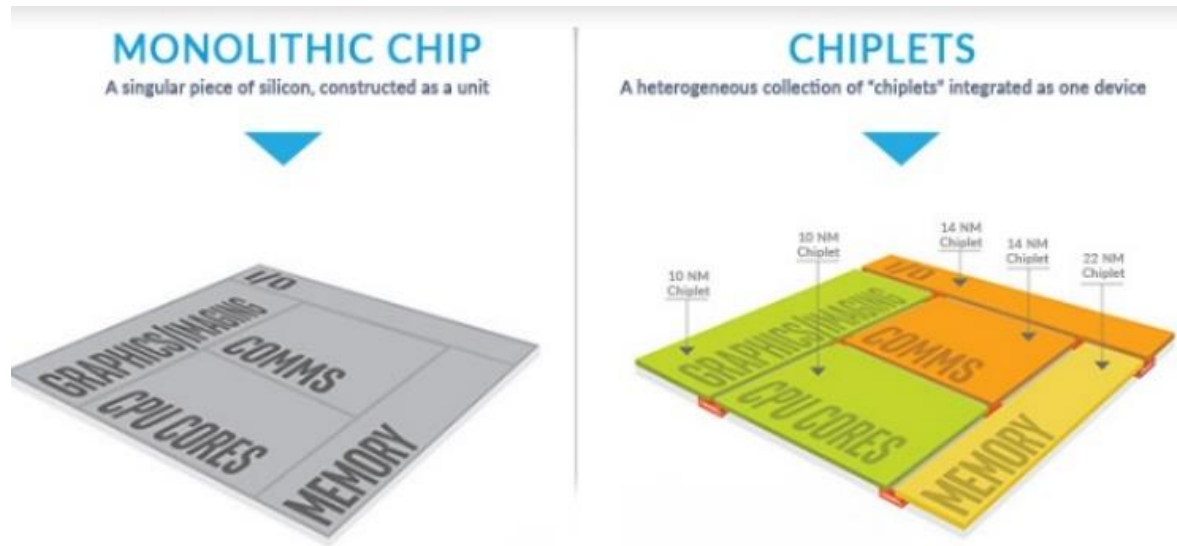


Figure (2) Standard monolithic chip architecture is compared to Chiplet architecture with a collection of partitioned subdivisions communicating under a single integrated device.

Chiplet Design: Due to the shortcomings of Moore’s Law, efficiency and economical solutions are needed to address future market challenges. Chiplets are designed to be the solution for the next few decades, as chiplets increase efficiency and cost-effectiveness in semiconductor die partitions. Although the exact mechanisms are trade secrets of chip designers, proprietary chip communication appears to be an integral aspect.

Stacked/3D Solutions: Because we are approaching the physical limit of transistor size, the industry is pushing to increase power, speed, and efficiency by expanding chip design in the 3rd dimension. One example includes stacked memory storage in 3D cache which reduces latency and increases bandwidth through shortened memory interconnections. This is analogous to city planning where developers have run out of space to develop property side by side within city limits. The only solution is to build vertical skyscrapers, and similarly, die manufacturer are looking to build stacked die and packing solutions.

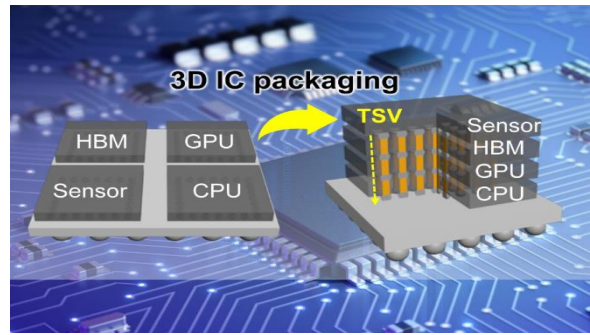


Figure (3) A comparison between 2D packaging and stacked solutions. Each sub portion of the IC is connected via vertical electrical connections (TSV- Through silicon via).

B. Growth Drivers and Market Opportunities

Several drivers stand out as primary catalysts for semiconductor market growth. Here are the most prominent:

Electric Vehicles (EVs): Chip growth will continue to see influence due to EV demand. Especially with the push towards hybrid and complete EV adoption, the industry should expect continued and steady growth in this segment. This market shows steady growth increasing market size by over 800% during this 10-year period.

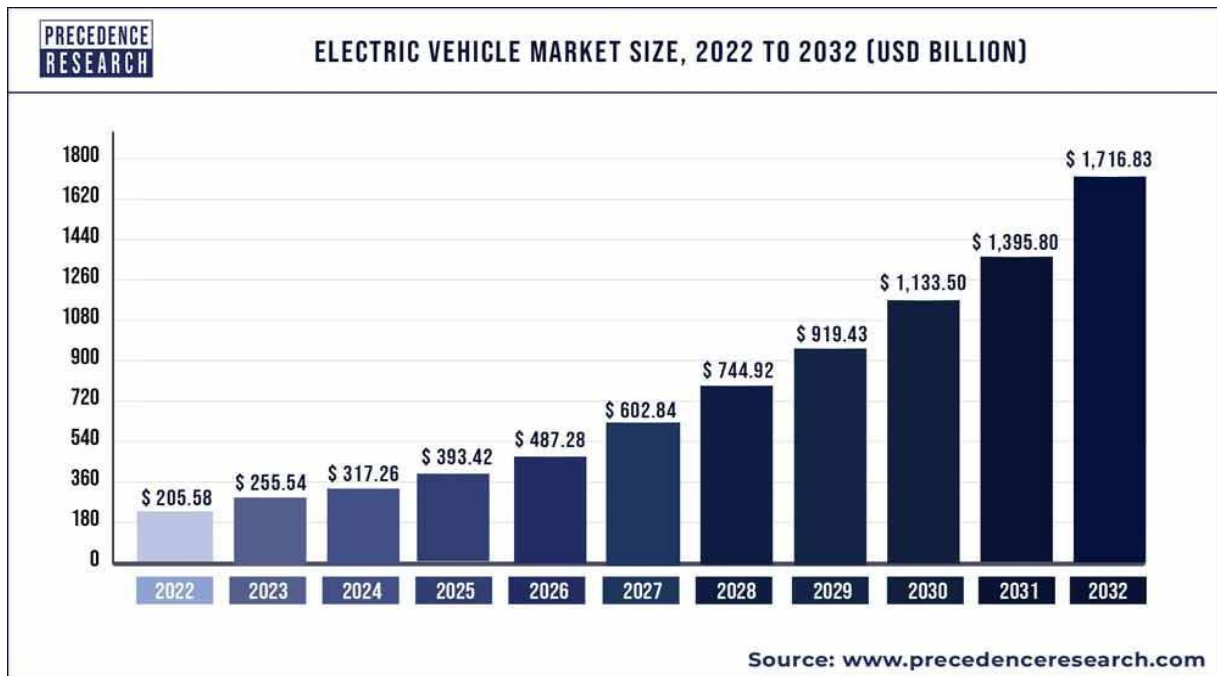


Figure (4) The forecast between 2022 and 2032 for EV market size is promising with a 23.1% CAGR.

Smartphone industry: Although 5G has not lived up to its promise due to lackluster speeds, poor deployment, and sub-optimal network connections³, steady growth in yearly smartphone shipments proves this market segment will remain an important growth driver. This market shows steady, yet slower growth than electric vehicles only increasing market size by 80%.

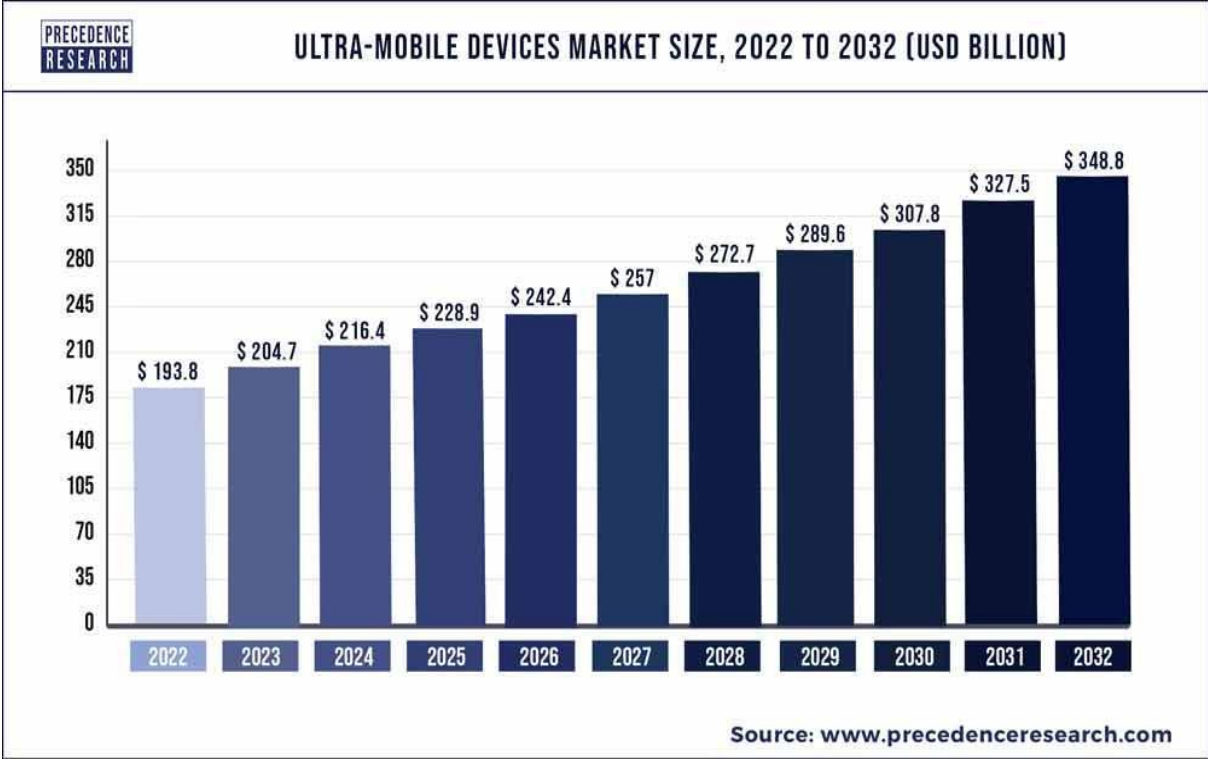


Figure (5) The forecast for mobile device market size is with a 6.1% CAGR between 2022 and 2032.

³ (5G in the US: Why the network of the future has not yet delivered on the revolution that we were promised)

Server and AI Expansion: Increasing reliance on cloud technologies drives server growth leading to an increased demand for faster and efficient semiconductors. Due to the recent boom in artificial intelligence, devices such as smartphones to autonomous vehicles require existing and new semiconductor technologies. Large server AI modeling and chat boxes such as chat-GPT require enormous amounts of computational power and efficiency. This market segment has promising potential as the technology matures and integration continues across interdisciplinary industries. This reliance requires transistor sizes that are expected to reach a 3nm process by 2024 and a 2nm process by 2026 for TSMC chips with Intel planning a 1.8nm process by 2025⁴.

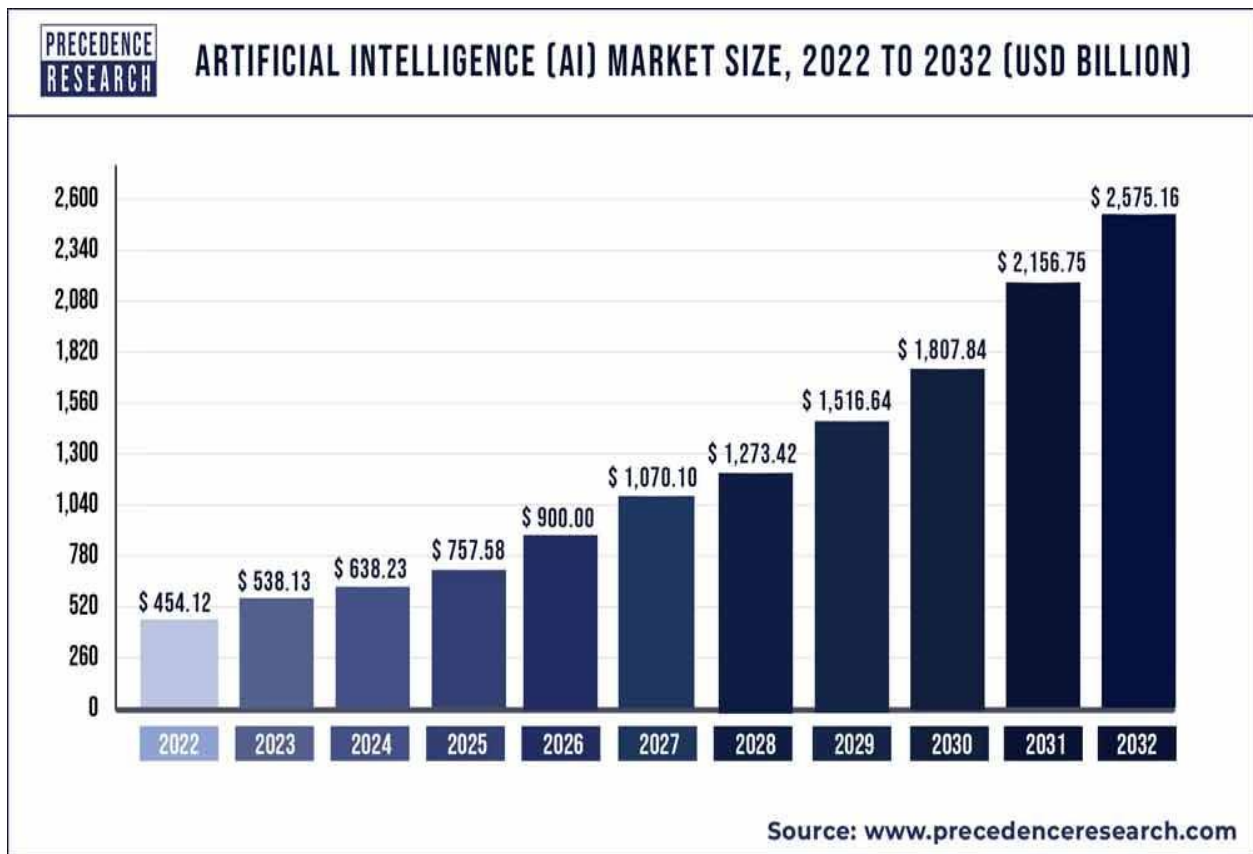


Figure (6) The forecast for artificial intelligence market size is promising with a 19% CAGR between 2022 and 2032.

⁴ (Intel plans for 18A chips by 2025 to challenge Samsung, TSMC dominance)

C. Global Markets

US investment has seen tremendous growth in recent years due to favorable investments from the current administration's CHIPS Act securing \$52 billion in subsidies⁵. These funds are being used for plant construction, workforce development, and long-term supply chain investments. Intel is spearheading this push, with plans to spend \$39 billion on new wafer fabrication sites and plant incentives to lead next-generation technology⁶. This investment is supplemented with Samsung, Entegris, Global Foundries, and other large domestic semiconductor companies. One example includes TSMC's new wafer fab in Arizona for advanced 5nm processes. The plant is expected to open by 2024 and will produce 20,000 wafers a month. TSMC plans to train Arizona University students in Taiwan to bring the Arizona plant up to speed⁷.

Europe remains relevant in the semiconductor market in specialized areas, notably automotive semiconductors, power electronics, and IoT applications. Due to global shortages of semiconductor chips and security concerns due to the recent Ukraine-Russian war, Europe is seen as risky for local investments. However, the EU has developed its own CHIPS Act attracting nearly \$90 billion in investments including packaging and testing facilities in Poland, and wafer fabs in Germany. TSMC alongside, Bosch, Infineon, and NXP commits €11 billion euros for a manufacturing plant to open in 2027 in Dresden. Additionally, Intel spends €30 billion euros in Magdeburg Germany⁸. These investments are examples of the EU bolstering their local manufacturing capabilities in Poland and especially Germany while combating geopolitical tensions.

The semiconductor manufacturing market in Asia holds a dominant position in the global landscape. Taiwan, South Korea, and China are at the forefront with their own plans for increasing market share. Taiwan's silicon chip manufacturing leader TSMC, and South Korea's Samsung, stands as two of the world's largest semiconductor foundries. Driven by the "Made in China 2025" initiative, China plans to reduce its reliance on imports by investing in research and development, manufacturing, and local supply chains⁹.

In summary, the semiconductor industry, supported by EV, Smartphone, and server/AI demands is undergoing transformative changes to increase manufacturing capacity. Due to US-China and other geopolitical conflicts, the semiconductor industry is focusing on global diversification. Not only do nations want to remove single-country manufacturing dependencies such as TSMC's dominance in Taiwan, but they also want to invest in domestic manufacturing/services.

⁵ ("FACT SHEET: CHIPS and Science Act Will Lower Costs, Create Jobs, Strengthen Supply Chains, and Counter China")

⁶ ("CHIPS for America")

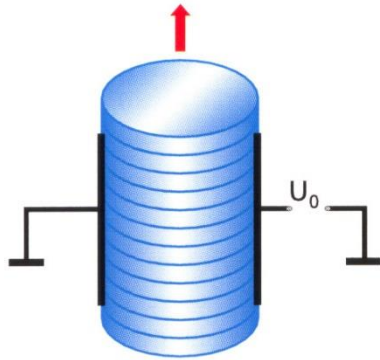
⁷ ("How ASML, TSMC And Intel Dominate the Chip Market")

⁸ ("European Chips Act")

⁹ ("SIA WHITEPAPER: TAKING STOCK OF CHINA'S SEMICONDUCTOR INDUSTRY")

III. Understanding Piezoelectric Actuators

A. Understanding the Piezoelectric Effect:



A clear grasp of piezo theory is needed to understand the utilization of piezoelectric technology within semiconductor manufacturing. The piezoelectric effect occurs when certain crystalline materials produce an electric charge when subjected to mechanical stress. The inverse of this phenomenon called the inverse piezoelectric effect, occurs when a material deforms due to an applied electric field. Originally utilized in ultrasonic systems, piezoelectric applications now extend to nanopositioning systems, grill lighters, and even guitar pickups.

Figure (7) A piezoelectric stack actuator made of stacked ceramic discs is shown. Electrodes are attached to either side and a voltage U_0 is applied. The direction of motion in the axial direction is highlighted in red.

B. Working Principle of Piezoelectric Actuators:

Piezoelectric actuators utilize the inverse piezoelectric effect in the application of piezo stacks made of stacked ceramic discs that are laminated and connected in parallel. When utilizing materials such as PZT (lead-zirconate-titanium), these piezo stacks will expand in the axial direction of the stack with an applied electric field. The current applied to the stack deformation predominantly determines the speed of the piezo stack operation. Piezo stack design allows customization such as incorporating a central hole to encourage airflow or if access is needed. These piezo stacks can be constructed as bare stacks, encased stacks with a mechanical preload, or integrated into other designs such as a multi-axis stages with the addition of flexure hinges to translate high-motion profiles.



Figure (8) Examples of various piezoelectric products (From left to right): A collection of piezoelectric stacks with varying degrees of lengths and diameters, a piezoelectric objective positioner used for objective autofocusing, and a piezoelectric stage positioner used for wafer chuck handling.

C. Advantages:

- Maintenance: Piezos do not require any maintenance once installed.
- Precision: Step sizes are often sub-nanometer and only limited by the noise characteristics of the voltage supply.
- High Compressive Strength: Piezos are stiff ceramic materials that can withstand high compression forces and ensure long-term usability. Precise construction and adhesives increase this compressive capability.
- Lifetime Durability: Piezos used under proper environmental conditions will last billions of cycles. The piezoelectric distortion does not damage the ceramic.
- Environment Compatibility: Piezos are non-magnetic and will not interfere with electromagnetic systems or introduce excess magnetic fields. Also, piezos are operable in vacuum environments.
- Solid-State Design: Due to the solid-state design, there is practically zero internal friction or stress. This limits the possibility of mechanical/electrical failure.
- Rise Time: Piezos have very fast rise times- as low as microseconds due to the high resonant frequency properties.
- High force Output: There are two force outputs of piezos. The blocking force is the maximum force applied with zero stroke and the acceleration force is due to dynamic motion. Both are high and contribute to excellent dynamic properties.
- Actuation Speeds: Piezos are recommended up to 80% of their resonant frequency, which in some cases is as high as 10's of kHz¹⁰.
- Amplified Motion: Actuator amplitudes can be increased due to leverage transmission systems such as parallelogram flexure hinge design and dual stack configurations in precision stages.

D. Disadvantages:

- Hysteresis and Creep: After an initial displacement due to residual polarization from ferroelectric properties, a smaller additional motion occurs over a longer time scale, known as creep. Also, PZT ceramics exhibit a hysteresis curve, where the voltage step applied does not directly correlate with the deformation observed. These disadvantages are not problematic with highly dynamic motion since neither drift nor creep has enough time to take full effect.
- Risk of Depolarization: Actuator performance varies with very high temperatures. Heating beyond the Curie Temperature of 150-200°C, which is the temperature at which piezoelectric materials lose their defining properties, results in the loss of piezoelectric characteristics.
- Tensile and Torque forces: Although piezoelectric stacks are excellent at withstanding compressive forces, they are fragile when subject to large tensile forces and will shatter.
- Cost: Due to the advanced manufacturing techniques required to build and design piezos, ceramic costs, and ultra-precise electronics, piezos are often a costly option. The voltage noise required for piezo controlled electronics needs to be very small to maintain the small voltage steps needed for precise actuation. Additionally, these electronics are often analog and require high amperage/bandwidth requirements which increases electronics costs.

¹⁰ (Newport)

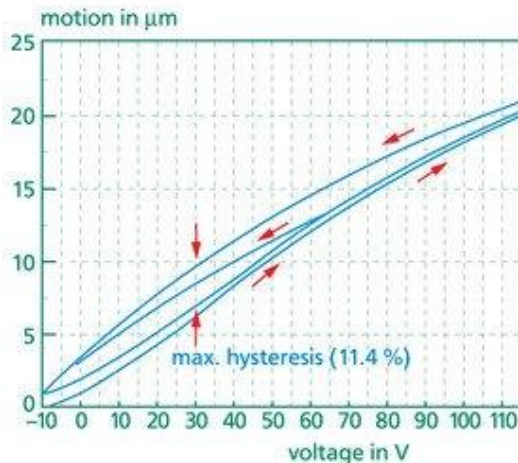


Figure (9) Displacement vs voltage is plotted to represent recorded motion of a stack actuator. Hysteresis is observed and accounts for 11.4% difference in observed motion. Red arrows demonstrate hysteresis progression.

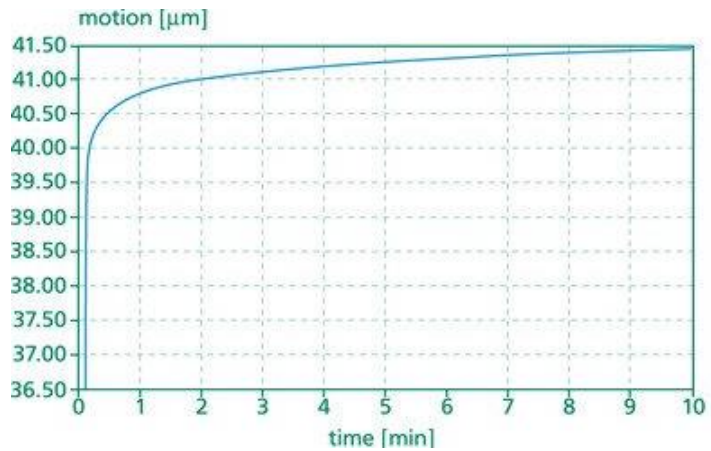


Figure (10) Creep is shown for a stack actuator over a period of 10 minutes. The majority of the additional motion is observed within the first decade of time. The measured position is typically within 1-2% of the total stroke.

E. Solutions to piezoelectric disadvantages:

Closed-loop measurement systems and software algorithms are a practical solution to overcome hysteresis and drift. A measurement device will record the measured position of the device and compare it against the anticipated position. The system will introduce iterative changes to the input signal that increase the precision and repeatability of piezoelectric systems to single-digit nanometer values or below. Additionally, if a piezo must be subject to temperatures close to its Curie Temperature, cooling via forced air or liquid cooling is recommended. Finally, preloading a piezo stack with a mechanical load is an excellent way to withstand tensile or torque forces. This will help ensure reliable lifetime operation for the end user and is especially useful for dynamic applications. Integrating dual stack design into piezo stages will also increase load capacity and withstand tensile forces while keeping a small form factor. These dual stack designs and increased preloading will allow inverted and custom installation of the piezo.

Overall, incorporating piezoelectric systems into semiconductor manufacturing presents many opportunities, from precision positioning of manufacturing components, to process improvement and simplification. Semiconductor manufacturers utilize the advantages of piezoelectric systems to increase precision, accuracy, and process efficiency with a compact and versatile solution. The following section expands on these applications with detailed examples of many semiconductor manufacturing steps.

IV. Applications of Piezoelectric Systems in Semiconductor Manufacturing Steps

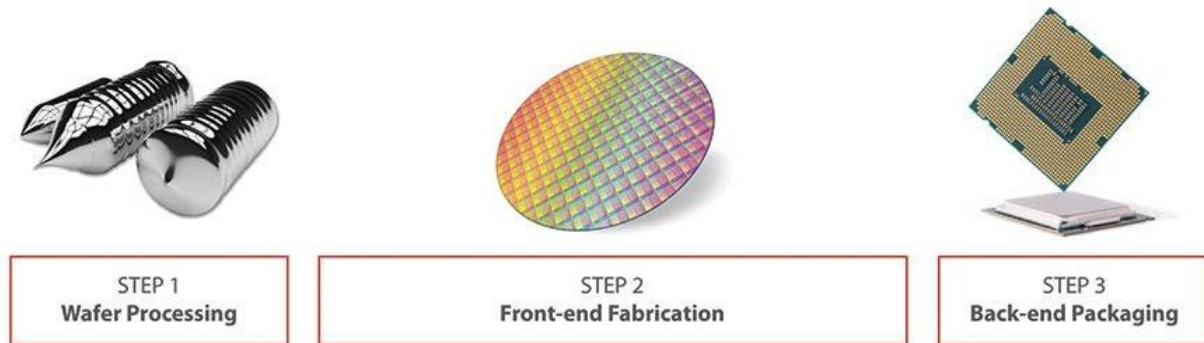


Figure (11) Each significant step of the semiconductor manufacturing process is shown. Silicon ingots are processed into wafers during step 1, dice are fabricated during the front-end of the process, and finally dice are packing into packaged device during back-end packaging.

A. Wafer Processing (From Silicon to Wafer)

Silicon ingots are the foundation of semiconductor manufacturing processes serving as the primary material for producing silicon wafers. Known as the Czochralski crystal growth process, silicon ingots begin as seed crystals and are fabricated into rigidly long ingots. This process transforms polycrystalline silicon with excellent thermal and optical properties to monocrystalline silicon with higher conductivity and electrical properties that are better suited for the semiconducting manufacturing process. The wafer fabrication process is summarized as a series of continuous steps. First, a small silicon crystal called a seed is prepared in a crystal puller. Polycrystalline silicon is then heated in a furnace until it becomes liquid silicon. The seed crystal is immersed into the molten silicon and slowly pulled upwards until a singular-crystal ingot is formed (monocrystalline silicon). Dopants such as boron or phosphorous are added to impart desired electrical properties. The ingot is cooled, annealed, and remains a fully formed ingot. A diamond wire saw segments the silicon ingot into thin discs known as wafers. Finally, each silicon wafer is polished with mechanical and chemical techniques to ensure smoothness and evenness. The silicon wafer is now ready for die fabrication.

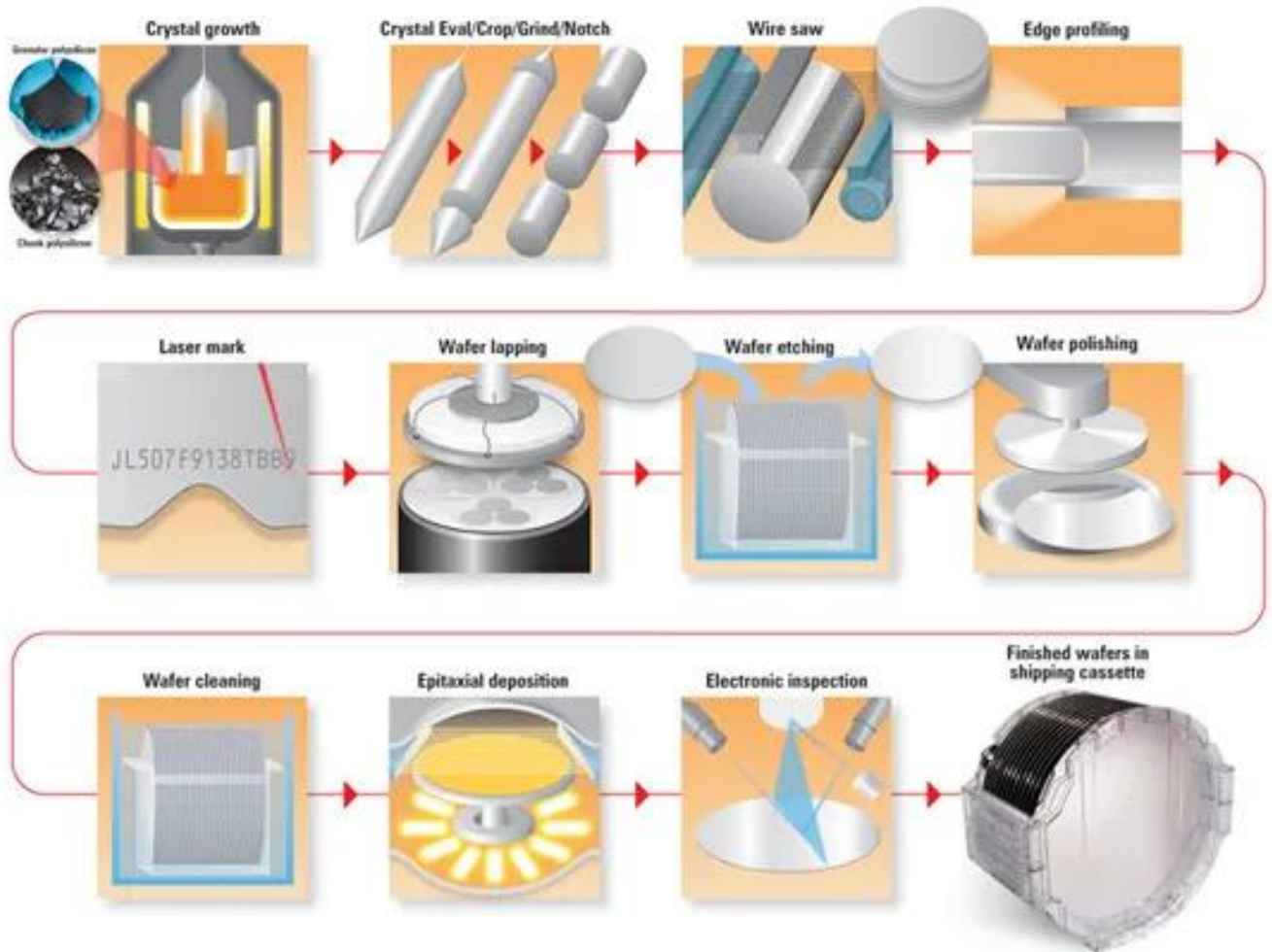


Figure (12) The wafer fabrication process from crystal growth to finished wafers. Smaller sub steps, such as laser mark, wafer lapping and etching are shown. Key steps to highlight for piezoelectric system applications are the first four steps: Crystal growth, crystal grind, wire saw, and edge profiling, as well as wafer polishing and electronic inspection.

Piezoelectric systems are utilized during the slicing and polishing steps of wafer fabrication and are particularly useful in wafer inspection and reduction of wafer warpage due to process irregularities caused by temperature fluctuations or uneven material deposition. During the slicing process, wafer thicknesses can vary from 280 micrometers to 725 micrometers¹¹. Advanced solutions are required to maintain a consistent and precise thickness. Piezoelectric objective lens positioners are solid-state systems free from internal friction and vibrations proving excellent autofocusing solutions for microscopy. In traditional systems that do not include a piezoelectric objective positioner, internal friction could increase wear and tear of the system, and vibrations could cause imaging instability. Since piezo objective positioners offer up to 725 micrometers of travel with sub-nanometer resolution the entire depth of the wafer can be monitored dynamically with only piezo expansion without additional mechanical components creating vibrations. When integrated as part of a feedback control system, these positioning systems allow for real-time adjustments with fast and accurate operation. This ensures that the wafer is sliced uniformly across

¹¹ (Microchemicals)

the entire diameter, and if wafer defects are found not, these are immediately imaged and reported for continuous process improvements. Once the wafer is sliced, piezoelectric actuators can control a polishing instrument onto the silicon wafer. Applied actuator pressure on the surface of the silicon wafer leads to improved surface smoothness and reduces defect densities and wafer warpages.

B. Front-end Fabrication (From Wafer to Die)

Once the wafer has been fabricated after individual wafers have been cut, polished, and shipped, individual dice needs to be produced on the wafer at die fabrication facilities. This is a complex process that has many steps and sub-steps that maximize the total number of dies produced per wafer with minimal defects or errors and reduces process length. An integral step of die fabrication, and one of the most well-known is photolithography. Semiconductor photolithography enables circuit patterns to be transferred onto silicon wafers. This process begins when a polished wafer is coated with a light-sensitive layer called photoresist. The desired circuit pattern called the mask is aligned over the photoresist while ultraviolet (UV) light is shone, altering the coated photoresist. After the wafer is exposed to UV light, specific parts of the photoresist are removed and reveal the pattern. Here, the exposed areas are etched to create the desired circuit pattern.

As highlighted by chiplet significance and 3D chip solutions, the lithography process is repeated many times with multiple layers. The most developed solution is EUV lithography which utilizes extreme UV light to reach the most precise circuit patterns and compact transistor densities. Although Nikon and Canon are large manufacturers of older semiconductor lithography machinery, ASML is the only manufacturer of the latest machinery and has produced two distinct generations used today: Deep Ultraviolet lithography (DUV) down to 12 nm structure size, and Extreme Ultraviolet (EUV) down to 3 nm structure sizes. These are some of the most advanced technologies in the world with ASML having built complex supply chains that include nearly 800 suppliers¹². It is no surprise these machines require extreme precision, long-term durability, and repeatability for every component.

Few piezo stacks or objective positioners are currently being implemented in the latest generation of EUV machines due to the preference for voice coil or linear drive technology. However, piezos have been integrated into DUV lithography machines for many years mostly for short-stroke actuation for fine placement tasks. There are many mirrors and positioning tools that require precise and fast actuation that require single-digit nanometer repeatability or else defects will occur, ultimately lowering die yield. The best application of piezo technology in DUV lithography is using 3-dimensional positioning stages to align 300mm wafers on wafer chucks. This requires the nanopositioning of heavy loads up to 20kg with sub-nanometer resolution. The chuck will be used to



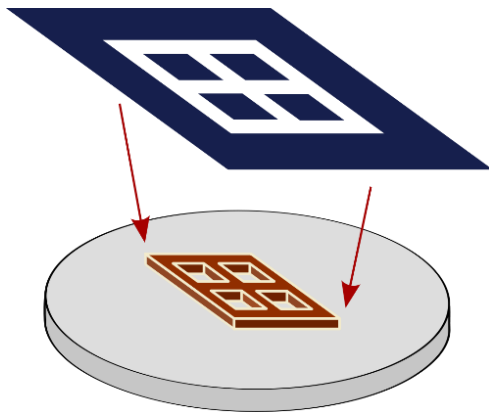
Figure (13) An ASML EUV lithography machine is shown. This is a complex machine with thousands of individual components originating from over 800 suppliers

¹² ("Statutory Interim Report")

quickly orientate the wafer during various steps in the lithography process and any deviation from a perfect alignment will produce defects that will later need to be inspected and removed from the total die yield.

A new application of piezo technology is used during the deposition phase of die fabrication, specifically chemical vapor deposition machinery (CVD). As different photoresist layers are being deposited onto the silicon wafer, chemical vaporizers are used to heat and effectively spray sub-micron-thick layers onto the silicon wafer. As photoresist processes become more advanced, the deposition process requires faster and thinner deposition layers. Therefore, the chemicals sprayed onto the wafer need to be finely vaporized requiring fast, precise, and consistent delivery systems. One way to develop a delivery system is by using compact stack actuators as the valve device within the chemical plumbing. These actuators are used for fast actuation that can be operated for hours at a time without wear or misalignment.

The applications with the highest potential for piezoelectric system implementation are inspection and defect inspection systems. For inspection use, objective positioners will autofocus the desired target to ensure proper alignment and placement, while locating potential defects. Objective positioners extend microscopy inspection by ensuring a sub-nanometer resolution with a total travel range of several hundred microns and several hundred-gram loads. Dynamic applications are possible due to fast scanning with resonance frequencies of several hundred Hz. Additionally, high load capacity stages offer nanometer level resolution to adjust the wafer chuck if optical inspection is not used. There are three main inspection areas these systems improve: Mask inspection, mask defect inspection, and E-beam inspection machines.



1. Mask inspection: The mask contains intricate circuit patterns that require a high-quality and flawless stencil made of glass or fused silica with an opaque film that needs to be projected onto wafers precisely¹³. For effective mask inspections, piezoelectric objective positioners can achieve rapid, high-resolution scanning across the entire mask to detect tiny discrepancies in mask production that may be overlooked with standard microscopy methods. These masks are scanned before being applied to the wafer.

Figure (14) A simplified illustration showing a photomask applied to a wafer in grey. The blue rectangle is the stencil, while the white opaque shape is the projected circuit pattern shown in brown.

¹³ ("Photomask")

2. Defect inspection: Once the mask projects the pattern to the wafer, the pattern needs to be free from defects or inconsistencies. High-resolution and fast-dynamics are needed to ensure defects are detected early in the process before multiple layers are projected which will cause major disruptions in downstream performance. The defects could include discrepancies between the expected pattern and the observed pattern on the wafer post-mask inspection. These defects are not solely due to circuit design defects, but discrepancies created due to the transfer of the mask onto the wafer.

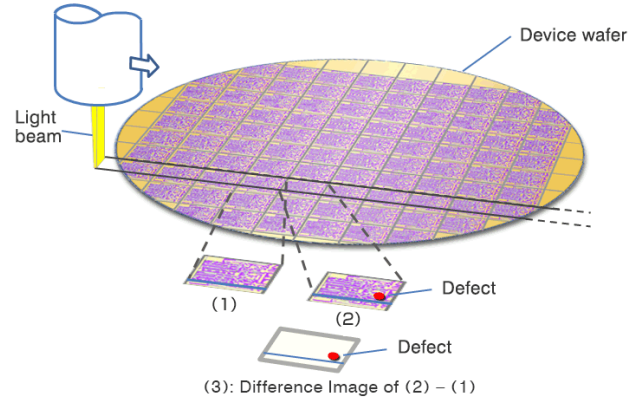


Figure (15) A wafer(yellow) containing hundreds of dice with photomasks applied in purple. A light source is projected for defects within the dice to be located. Defects are often compared against each other to identify the difference in circuit patterns.

3. E-beam inspection: With the development of smaller chip architectures, lithography patterns become smaller and harder to inspect. E-beam machines utilize electron beams to project onto the smallest section of the die that optical inspection tools cannot detect. These sensitivities are often smaller than 1nm and can be supplemented with piezo wafer positioners to align the electron beam to the dice. Objective positioners can be implemented to adjust objectives used in the E-beam apparatus. Often this is used in R&D machines separate from in-line manufacturing processes to solve current problems on the manufacturing line.

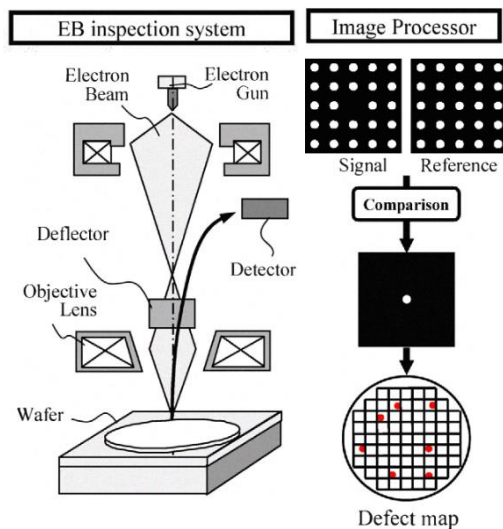


Figure (16) A simplified E-beam inspection system is divided into sub-components (left), and the E-beam imaged defects are shown(right). A standard E-beam system is composed of an objective and wafer handling system, both applications of piezo systems. Defects are imaged according to a reference and recorded signal.

These positioning tools are used to inspect dice manufactured during the semiconductor process. These tools increase precision, reduce defect analysis time, and improve process output. One final application during die fabrication is vibration control across various inspection steps. Electrical noise and vibrations are generated during operation. To reduce additional defects or abnormalities due to environmental noise or vibrations, piezoelectric actuators can be used. Similar to a noise cancellation effect, actuators are utilized by introducing an input actuation to mitigate feedback during machinery operation. These actuators are miniaturized and can actuate between 5-70kHz for long time periods further minimizing process interruptions or defects.

Overall, die fabrication is a lengthy step in the semiconductor manufacturing process that includes many interconnected processes such as lithography, inspection, and defect analysis. These systems combat many of the processes challenged with a miniaturized, and efficient solution via stack actuators or objective positioners.

C. Back-end Packaging (From Die-completed device)

Once semiconductor wafers have been processed and the die has been cut in a process called dicing, the die moves to the packaging step of the manufacturing process. Packaging serves to protect the die from environmental factors, connect the die to circuitry to communicate with external circuits or motherboards, dissipate heat during operation, and finally integrate into advanced packaging solutions such as multi-chip packages (MCP) or system-in-package (SIP)¹⁴. Once packaged, the device is tested to ensure functionality and performance. Finally, these devices are ready to ship and integrate into a vast array of electronic products, such as smartphones, electric cars, and medical devices. This is the final step to transform delicate silicon chips into robust components for real-world applications. Aside from potential positioning applications in this phase, piezoelectric systems can be utilized effectively in two main areas: fine-pitch bonding during packaging, and device cleaning due to advanced packaging structures.

Wire bonding is a critical step during packaging that connects individual dies to external circuitry linking the micro-scale of the semiconductor devices to the macro-scale of electronic devices. After dicing, individual dies are attached to a lead frame that serves as the device's structural and electrical interface. During this process, fine wires made of aluminum or gold are connected from design points on the die to points on the lead frame. Since this is a delicate process analogous to microscopic soldering, fine bonding must occur without any additional materials added which would otherwise render the circuit compromised. Ultrasonic energy must be used to create a metallurgical bond that is durable and miniature. Piezoelectric actuators can generate ultrasonic frequencies to facilitate this process ensuring precision, repeatability, and reliability. Once bonded, various protective molds are added to avoid environmental damage. These actuators are miniature and can produce high repeatability ultrasonic signals with highly tunable frequency responses to encourage varying degrees of wire bonding.

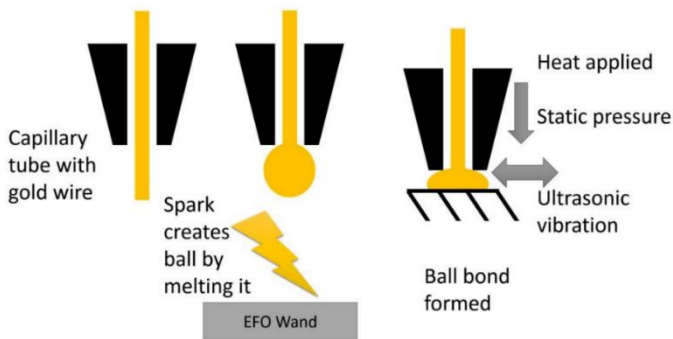


Figure (17) Here a simplified wire bonding process is shown in three steps. First a gold wire is placed in a capillary tube. Then, a spark is created by an EFO (electric flame off) wand which melts the gold wire into a sphere. Finally, with applied heat and sonic pressure, an ultrasonic vibration is introduced to form a bond between the spherical gold ball and the substrate.

Packaged device cleaning processes are integral to various steps of the semiconductor industry. The cleaning and preparation of surfaces involves removing unwanted particles, features, and structures using a variety of materials, processes, and equipment. To scale features and explore more efficient cleaning methods, new applications of existing technology are needed to address these issues. This involves cleaning immediately after wafer processing, die slicing, and during packaging.

One example during the production of advanced memory structures includes the challenge of cleaning confined hidden surfaces. 3D NAND and deep DRAM capacitors are examples of structures that include increased hidden layers and aspect ratios that disrupt high-volume manufacturing¹⁵. 3D NAND are

¹⁴ (Burkacky et al.)

¹⁵(Hars)

stacked flash memory devices that hold more memory storage than traditional 2D devices thanks to the implementation of 3D surfaces. Companies have introduced bubble oscillation technologies to address these challenges. These technologies introduce controlled bubbles to clean hard-to-reach areas due to precise control of bubble cavitation. Features are not damaged during cavitation which reduces failure rates and increases cleaning throughput making it suitable to clean advanced 3D structures and high aspect ratios.

High-powered piezoelectric actuators and shakers are a potential solution to increase the success of bubble cavitation technologies¹⁶. Due to precise actuator signal outputs, compact device size, and lifecycle, piezoelectric shakers are a potential solution for these technologies. Although these processes tend to use a megasonic frequency range, piezoelectric actuators and shakers are capable of reaching a smaller bandwidth, but within a more precise frequency domain. This improves the cavitation process productivity and efficiency to address device scaling, complex structures, and the integration of new materials. Device cleaning is a critical process in various steps in the semiconductor manufacturing process to remove residual particles, prevent defects, and guarantee chip production efficiency.

There is a compelling case for integrating piezoelectric systems into post-wafer processing and device fabrication due to precision, reliability, and versatility. As the industry grapples with new complexities of 3D structures, high aspect ratios, and other challenges, the precise frequency generation and reliability of piezoelectric technology may provide solutions to back-end packaging for the semiconductor manufacturing industry.

Section V. Challenges and Considerations

Piezoelectric technology has made significant progress in advancing precision, durability, and reliability in semiconducting manufacturing. Integrating this technology does not come without its challenges. Operational factors, integration and compatibility with existing equipment, and cost-benefit analysis all need to be considered to fully assess this technology's challenges.

While piezoelectric systems offer sub-nanometer precision, this technology does operate under certain environmental and mechanical constraints. First, ceramic materials must not be heated past their Curie temperature (150-200°C), or their piezoelectric properties will be diminished. In high-temperature environments, this requires the addition of forced air or non-water liquid to be introduced for active cooling. In some cases where space is limited this may introduce additional complexity and spatial requirements. Additionally, piezoelectric systems will need special adaptations to operate under vacuum or clean room requirements. Luckily the ceramic will function fine in vacuum, however, cables/leads will have to be replaced with materials that do not off-gas and increase the ultra-low vacuum pressures.

The push towards smaller structure sizes results in higher technical requirements that are far beyond resolution improvements. Since semiconductor processes require precision imaging, all symmetry aspects of nanopositioning optics must be accurate. This includes straightness of motion, cross-axis motion, and lateral run-out. The entire motion profile of a piezo system must have improved linearity so there is minimal drift of the desired set position. This will require measurement systems in closed-loop configurations that have the highest linearity properties which could induce additional costs. For extreme cases, linearity may need to be improved beyond what closed-loop systems could provide, and collaboration between piezo manufacturers and semiconducting firms must be encouraged so that piezo products are optimized. Luckily, piezo systems are extremely durable, so once introduced, are expected to

¹⁶ (Wang and Lei)

last the entire lifetime of the manufacturing instrument. Proper installation is imperative because piezo electrodes may drift into the ceramic during dynamic conditions. This is due to a constant electric field during operation and a large number of technical aspects need to be considered that are contributed from installation and the operating environment.

With the addition of any technology, attention needs to be paid to integrating piezoelectric technology into current semiconductor equipment to ensure seamless integration. This includes retrofitting existing nanopositioning technology, ensuring electric capability, and examining potential points of failure with new interfacing requirements. The initial investment required for piezoelectric implementation must be considered and the financial implications cannot be overlooked. Piezoelectric technology does improve yields and increases precision, and equipment durability which leads to significant long-term savings. However, these long-term savings must be analyzed to assure the timeline aligns with business objectives.

Section VI. Conclusion

Piezoelectric technology has seen recent success in the semiconductor manufacturing industry, yet has not fully captured the full potential of implementation. As the push for chip miniaturization continues, and equipment processes require machinery miniaturization, piezoelectric actuator technology continues to evolve offering greater precision and miniaturization. Improvements in ceramic materials, flexure hinge design, and electronics integration are expected to increase integration into more challenging environments requiring smaller form factors, efficiency, and intricate tasks. Manufacturers of piezo systems operate at the limit of mechanical and material properties to develop the next level of high-precision positioning tools. A deeper investigation into piezo theory is not necessary, however, experts in materials science and mechanical systems should collaborate to push the limits of static and dynamic positioning applications. As piezoelectric technology evolves, it leads to further streamlined processes previously deemed unfeasible. With the intricate evolution of 3D chip designs, and multi-layer chip architectures, the precision of piezoelectric systems may become foundational. These advancements and integration capabilities are not merely a trend, but a cornerstone of future development.

As the semiconductor industry advances into a new era founded on further chip miniaturization, and increased focus on efficiency, piezoelectric systems are at the forefront of this advancement bringing the gap between precision and reliability once thought unattainable into real-world applications. Piezoelectric systems offer viable solutions to many challenges in the semiconductor manufacturing steps such as ingot slicing, defect analysis systems, and fine-pitch bonding solutions. The capabilities of this technology provide precision at the sub-nanometer scale enhancing wafer preparation, chip imperfections, and advanced packaged solutions. While the decline of Moore's Law may impact the industry in new ways rarely seen before, piezoelectric technologies emerge as a readily available and future-forward solution to address complex modern challenges at the intersection between materials science and mechanical engineering. Due to the complexity of semiconductor manufacturing, and application specific technical requirements for piezo technology, further collaboration between semiconductor and piezo manufacturers is needed to ensure the semiconductor industry continues to innovate and push the boundaries of chip miniaturization.

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